Sub A1

WHAT IS CLAIMED IS:

1. An integrated circuit having a plurality of circuits formed on a common substrate that are isolated by isolation regions in said common substrate between said circuits, said integrated circuit made by the process of:

masking predetermined locations of said common substrate that are aligned with said isolation regions with a material that is capable of masking high energy ions;

irradiating said common substrate with said high energy ions such that said high energy ions have an energy level sufficient to implant said high energy ions in embedded regions of said common substrate that are substantially aligned with unmasked portions of said common substrate that are aligned with said circuits so that said isolation regions are formed in said common substrate between said embedded regions and said embedded regions are buried in said common substrate so that a portion of said common substrate separates said embedded regions from said circuits.

2. An integrated circuit comprising:

a common substrate having low doping and a first predetermined resistance;

circuitry formed on predetermined portions of said common substrate;

embedded regions of said common substrate that are implanted with ions such that said embedded regions have a resistance that is lower than said first predetermined resistance, said embedded regions being substantially aligned with said circuitry and buried in said common substrate so that a portion of said common substrate separates said embedded regions from said circuitry.

3. The integrated circuit of claim 2 wherein said common substrate includes an epitaxial layer and a substrate layer.

4. The integrated circuit of claim 2 wherein said embedded regions form a checkerboard pattern.

5. The integrated circuit of claim 2 wherein said implanted ions comprise boron ions.

6. The integrated circuit of claim 2 wherein said implanted ions comprise phosphorous ions.

Sub A2

7. A silicon wafer suitable for the formation of integrated circuits comprising:

a common substrate on which said integrated circuits can be formed in predetermined locations on said common substrate, said common substrate having a first predetermined resistance;

embedded regions of implanted ions deposited in said common substrate that are substantially aligned with said predetermined locations on said common substrate, said embedded regions having a resistance that is lower than said first predetermined resistance and buried in said common substrate so that a portion of said common substrate separates said embedded regions from said predetermined locations on which said circuits can be formed.

8. The silicon wafer of claim 7 wherein said common substrate includes an epitaxial layer and an underlying substrate layer.